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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,437	KIRK ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: According to MPEP § 608.01 (m), the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). The phrase "Claims" is not considered equivalent to these appropriate phrases. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the buffer". There is insufficient antecedent basis for this limitation in the claim.

Claim 16 recites the limitation "the raster operations". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Duluk 2 (US006771264B1).

6. With regard to Claim 1, Duluk 1 describes an application programming interface (Col. 5, lines 29-31) for a programmable graphics processor (Col. 5, lines 7-17; Col. 11, lines 64-65), comprising one or more program instructions (reorder logic, 2623-0, Figure 13b) within the programmable graphics processor (Col. 7, lines 40-41) to detect a position conflict for a position and prevent a subsequent access of the position until the position conflict is resolved (Col. 14, lines 12-40).

However, the program instructions described by Duluk 1 are for reordering the memory addresses to be accessed (Col. 14, lines 1-19), and Duluk 1 does not explicitly teach that these program instructions are for configuring a fragment processor. However, a related patent, Duluk 2, describes that OpenGL defines a set of per-fragment operations (Col. 6, lines 34-37), and these per-fragment operations determine the manner in which the pixels are stored (Col. 6, lines 42-65). Therefore, Duluk 2 describes one or more program instructions to configure a fragment processor, and these per-fragment operations determine the manner in which the pixels are stored.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Duluk 1 so that the program instructions are for configuring a fragment processor as suggested by Duluk 2 because Duluk 2 suggests that this is needed in order to determine the manner in which the pixels are stored (Col. 6, lines 34-37, 42-65), and also to perform various tests on the fragments, such as the ownership test, scissor test, alpha test, color test, stencil test, depth buffer test, to determine what operation needs to be performed on the fragment to modify the pixel in the frame buffer at that location (Col. 7, lines 8-22).

7. With regard to Claim 2, Duluk 1 describes that a program instruction (2623-0, Figure 13b) receives memory addresses, and for each memory address received, conflict detection block (2602) determines if a memory conflict is likely to occur based upon the addresses contained in first level reorder queue (2603) (Col. 14, lines 12-40). In order to determine if a memory conflict is likely to occur, the addresses received by a program instruction must inherently include a source location and a destination location.

8. With regard to Claim 3, Duluk 1 describes that the source location includes a buffer identifier corresponding to one of several buffers (Col. 12, lines 2-23).

9. With regard to Claim 4, Duluk 1 describes that the destination location includes a buffer identifier corresponding to one of several buffers (Col. 12, lines 24-41).

10. With regard to Claim 5, Duluk 1 describes that the destination location contains fragment data including at least one of depth, color, and stencil (Col. 8, lines 19-28; Col. 9, lines 30-45).

11. With regard to Claim 6, Duluk 1 describes a method of processing program instructions (Col. 7, lines 39-46; 2623-0, Figure 13b; Col. 14, lines 12-40) comprising receiving a pixel load instruction including a source address corresponding to a location within the buffer (Col. 12, lines 2-23). The conflict detection block (2602, Figure 13b) detects if a memory conflict is likely to occur (Col. 14, lines 12-27). In other words, the conflict detection block detects a write to the source address is pending. The conflicting address request is sent to conflict queue (2604). The conflicting address request is a request to read data stored in the location corresponding to the source address (Col. 14, lines 12-40). A queue is a list that is accessed in a first-in, first-out manner, as is well-known in the art. Therefore, the conflicting address request will not be executed until after the previous pixel load instruction is complete. Therefore, Duluk 1 describes waiting to read data stored in the location corresponding to the source address until the write to the source address is complete (Col. 14, lines 12-27).

However, Duluk 1 does not explicitly teach that the program instructions are fragment program instructions. However, Duluk 2 describes fragment program instructions, as discussed in the rejection for Claim 1.

12. With regard to Claim 8, Duluk 1 describes that if a conflict with a previous request to load a pixel is determined, the conflicting address request, which is an additional program instruction (Col. 7, lines 39-46; Col. 11, lines 64-67), is sent to conflict queue (2604, Figure 13b; Col. 14, lines 12-27). A queue is a list that is accessed in a first-in, first-out manner, as is well-known in the art. Therefore, the additional program instruction will not be executed until after the previous pixel load instruction is complete. Therefore, Duluk 1 describes receiving additional program instructions after the receiving of the pixel load instruction; and waiting to execute the additional program instructions until the write to the source address is complete (Col. 14, lines 12-27).

However, Duluk 1 does not explicitly teach that the program instructions are fragment program instructions. However, Duluk 2 describes fragment program instructions, as discussed in the rejection for Claim 1.

13. With regard to Claim 9, Duluk 1 describes receiving additional program instructions after the receiving of the pixel load instruction, as discussed in the rejection for Claim 8. In one embodiment, the address requests in the conflict queue (2604, Figure 13b), which are the additional program instructions, are output to control circuit (2605). In this manner, the reordered address requests are applied to reordered address queue (2606) to access RAMBus

memory controller (2649) with fewer, and often times zero, conflicts (Col. 14, lines 27-40). Since there are now no conflicts, there is no need for the additional program instructions to wait until after the first pixel load instruction is complete to be executed. Therefore, Duluk 1 describes executing at least one of the additional program instructions before the write to the source address is complete (Col. 14, lines 12-40).

However, Duluk 1 does not explicitly teach that the program instructions are fragment program instructions. However, Duluk 2 describes fragment program instructions, as discussed in the rejection for Claim 1.

14. With regard to Claim 10, Duluk 1 describes that in one embodiment, the address requests in the conflict queue (2604, Figure 13b), which are the subsequent program instructions, are output to control circuit (2605). In this manner, the reordered address requests are applied to reordered address queue (2606) to access RAMBus memory controller (2649) with fewer, and often times zero, conflicts (Col. 14, lines 27-40). Since there are now no conflicts, there is no need for the additional program instructions to wait until after the first read request is complete to be executed (Col. 14, lines 34-40). Therefore, Duluk 1 describes executing at least one subsequent program instruction while waiting to read the data stored in the location corresponding to the source address (Col. 14, lines 12-40).

However, Duluk 1 does not explicitly teach that the program instructions are fragment program instructions. However, Duluk 2 describes fragment program instructions, as discussed in the rejection for Claim 1.

15. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Duluk 2 (US006771264B1), further in view of Baldwin (US005815166A).

Duluk 1 and Duluk 2 are relied upon for the teachings as discussed above relative to Claim 6. Duluk 1 describes comprising storing the data read from the location corresponding to the source address (Col. 12, lines 3-41).

However, Duluk 1 and Duluk 2 do not teach storing the data in a register specified by the pixel load instruction. However, Baldwin describes a fragment processing pipeline (Col. 30, lines 37-52) comprising storing the data read from the location corresponding to the source address in a register specified by the pixel load instruction (Col. 11, lines 11-33; Col. 12, lines 13-15; Col. 13, lines 17-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Duluk 2 to include storing the data in a register specified by the pixel load instruction as suggested by Baldwin. Baldwin suggests that this must be done so that the data is written to the appropriate register (Col. 11, lines 30-33). Using registers improves data transfer rates (Col. 14, lines 63-67).

16. Claims 11, 12, 15-17, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Swanson (US005421028A).

17. With regard to Claim 11, Duluk 1 describes a fragment program for processing fragment data in a fragment processing pipeline (Col. 5, lines 14-17, 42-67), comprising a fragment

program instruction to write a destination location in a buffer (Col. 11, line 64-Col. 12, line 7); and a fragment program instruction to read the destination location in the buffer (Col. 11, lines 64-67; Col. 12, lines 20-23).

However, Duluk 1 does not teach that this is done without an intervening instruction to flush the fragment processing pipeline. However, Swanson describes processing primitive data in a processing pipeline (200, Figure 2; Col. 3, line 55-Col. 4, line 14), and writing and reading data in the buffer (212) without an intervening instruction to flush the processing pipeline (Col. 6, line 48-Col. 7, line 7; Col. 8, lines 33-64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Duluk 1 so that this is done without an intervening instruction to flush the fragment processing pipeline as suggested by Swanson. Swanson suggests that the time required for a single primitive to traverse the pipeline is called the pipeline latency, and this latency determines the duration of the pipeline flush. Such pipeline latency encountered during a pipeline flush removes the responsiveness and interactivity of the graphics system, and as input graphics primitives become more complex and the pipelines become longer, the pipeline latency problem grows. Moreover, since the current trend of graphics pipelines is towards higher level, more complex primitives which require more processing time in the pipeline, the penalty for a pipeline flush has become unacceptable if the computer graphics system is to function at high speeds. An alternative to pipeline flushing and resynchronization has thus become necessary for good system performance (Col. 2, lines 44-68).

18. With regard to Claim 12, Claim 12 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

19. With regard to Claim 15, Duluk 1 describes fragment program instructions to configure the fragment processing pipeline to perform raster operations (Col. 2, lines 21-25; Col. 6, lines 42-67).

20. With regard to Claim 16, Duluk 1 describes that the raster operations are performed using fragment data represented in a floating-point data format (Col. 2, lines 15-18, 21-25; Col. 8, lines 19-41).

21. With regard to Claim 17, Claim 17 is similar in scope to Claim 11, except that Claim 17 is for a computer program product having a computer readable medium having computer program instructions recorded thereon, the computer program product comprising the fragment program. Duluk 1 describes a computer program product having a computer readable medium having computer program instructions recorded thereon (Col. 5, lines 25-34), the computer program product comprising the fragment program (Col. 7, lines 39-46; Col. 11, lines 64-67). Therefore, Claim 17 is rejected under the same rationale as Claim 11.

22. With regard to Claim 21, Claim 21 is similar in scope to Claim 15, and therefore is rejected under the same rationale.

23. With regard to Claim 22, Claim 22 is similar in scope to Claim 16, and therefore is rejected under the same rationale.

24. Claims 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Swanson (US005421028A), further in view of Wood (US006204856B1).

25. With regard to Claim 13, Duluk 1 and Swanson are relied upon for the teachings as discussed above relative to Claim 11.

However, Duluk 1 and Swanson do not teach fragment program instructions to configure the fragment processing pipeline to perform depth buffering prior to shading. However, Wood describes fragment program instructions to configure the fragment processing pipeline to perform depth buffering prior to shading (Col. 1, lines 22-24; Col. 9, lines 64-67; Col. 12, lines 1-6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Swanson to include fragment program instructions to configure the fragment processing pipeline to perform depth buffering prior to shading as suggested by Wood because Wood suggests the advantage of reducing the number of attributes to be calculated (Col. 1, lines 62-64; Col. 11, line 62-Col. 12, line 6).

26. With regard to Claim 18, Claim 18 is similar in scope to Claim 13, and therefore is rejected under the same rationale.

27. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Swanson (US005421028A), further in view of Isard (US 20040207623A1).

28. With regard to Claim 14, Duluk 1 and Swanson are relied upon for the teachings as discussed above relative to Claim 11.

However, Duluk 1 and Swanson do not teach fragment program instructions to configure the fragment processing pipeline to perform depth peeling. However, Isard describes fragment program instructions to configure the fragment processing pipeline to perform depth peeling [0017, 0055].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Swanson to include fragment program instructions to configure the fragment processing pipeline to perform depth peeling as suggested by Isard because Isard suggests that depth peeling is needed to render shadows cast by transparent objects [0055].

29. With regard to Claim 19, Claim 19 is similar in scope to Claim 14, and therefore is rejected under the same rationale.

30. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duluk 1 (US006288730B1) in view of Swanson (US005421028A), further in view of Sen.

Duluk 1 and Swanson are relied upon for the teachings as discussed above relative to Claim 17.

However, Duluk 1 and Swanson do not teach that the fragment program includes fragment program instructions to configure the fragment processing pipeline to perform dual depth shadow mapping. However, Sen describes that the fragment program includes fragment program instructions to configure the fragment processing pipeline to perform dual depth shadow mapping (p. 522).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Duluk 1 and Swanson so that the fragment program includes fragment program instructions to configure the fragment processing pipeline to perform dual depth shadow mapping as suggested by Sen. Sen suggests that the most popular techniques for interactive rendering of hard shadows are shadow maps and shadow volumes. Shadow maps work well in regions that are completely in light or in shadow but result in objectionable artifacts near shadow boundaries. In contrast, shadow volumes generate precise shadow boundaries but require high fill rates. Dual depth shadow mapping is a hybrid between shadow map and shadow volume techniques, and it allows the shader to construct a piecewise linear approximation to the true shadow silhouette, improving the visual quality over the piecewise constant approximation of conventional shadow maps (p. 521, 522, 525).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner